



# SERVICE MANUAL

CLASS D/DSC TERMINAL

**DS-100 #02**

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## INTRODUCTION

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This service manual describes the latest service information for the **DS-100** CLASS D/DSC TERMINAL at the time of publication.

MODEL	TRANSCEIVER
DS-100 #02	IC-M401EURO IC-M401E IC-M503E

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

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## DANGER

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**NEVER** connect the terminal unit to an AC outlet or to a DC power supply that uses more than 16 V. This will ruin the terminal unit.

**DO NOT** expose the terminal unit to rain, snow or any liquids.

**DO NOT** reverse the polarities of the power supply when connecting the terminal unit.

**DO NOT** apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the terminal unit's front end.



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## ORDERING PARTS

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Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

### <SAMPLE ORDER>

1110003200 S.IC TA31136FN DS-100 MAIN UNIT 5 pieces  
8810006050 Screw Icom screw E7 DS-100 Rear panel 10 pieces  
Addresses are provided on the inside back cover for your convenience.

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## REPAIR NOTES

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1. Make sure a problem is internal before disassembling the terminal unit.
2. **DO NOT** open the terminal unit until the terminal unit is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the terminal unit is defective.
6. **READ** the instructions of test equipment thoroughly before connecting equipment to the terminal unit.

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# SECTION 1 SPECIFICATIONS

## ■ GENERAL

- Frequency coverage : 156.525 MHz (Ch 70) Rx only
- Mode : 16K0G2B
- Power supply requirement : 13.8 V DC (negative ground)
- Usable temperature range : -20°C to +60°C; -4°F to +140°F
- Current drain (at 13.8 V DC) : 1.0 A (approx.)
- Antenna impedance : 50 Ω (nominal)
- Output impedance (for testing) : 100 kΩ (nominal)
- Dimensions (projections not included) : 165(W)×110(H)×78(D) mm; 6½(W)×2⅓(H)×5¼(D) in
- Weight : 1 kg, 2.2 lb (approx.)

## ■ RECEIVER

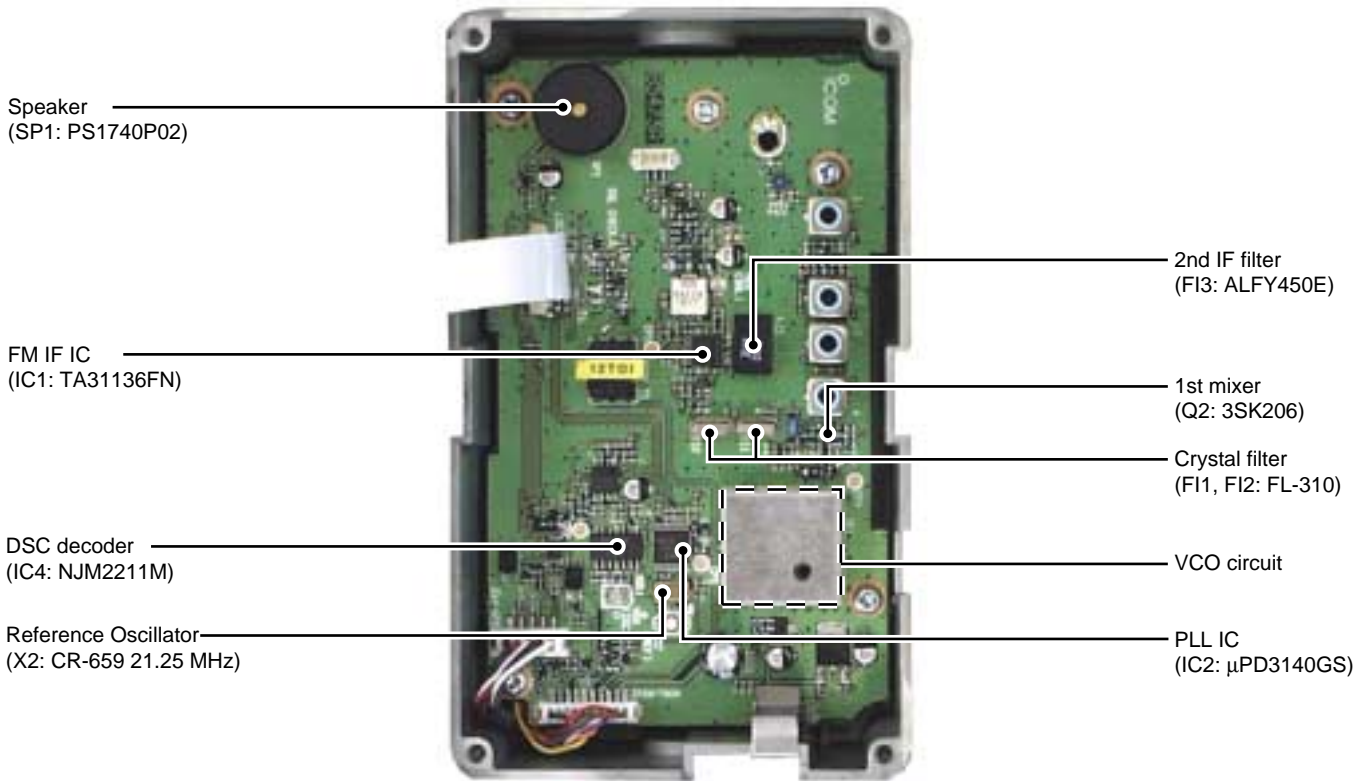
- Receive system : Double conversion superheterodyne system
- Intermediate frequencies : 1st 21.7 MHz  
2nd 450 kHz
- Sensitivity : 0 dBμ typical at 12 dB SINAD
- Adjacent channel selectivity : 70 dB
- Spurious response : 70 dB
- Intermodulation rejection ratio : 68 dB
- Hum and noise : -40 dB

Specifications are measured in accordance with EN301-025.

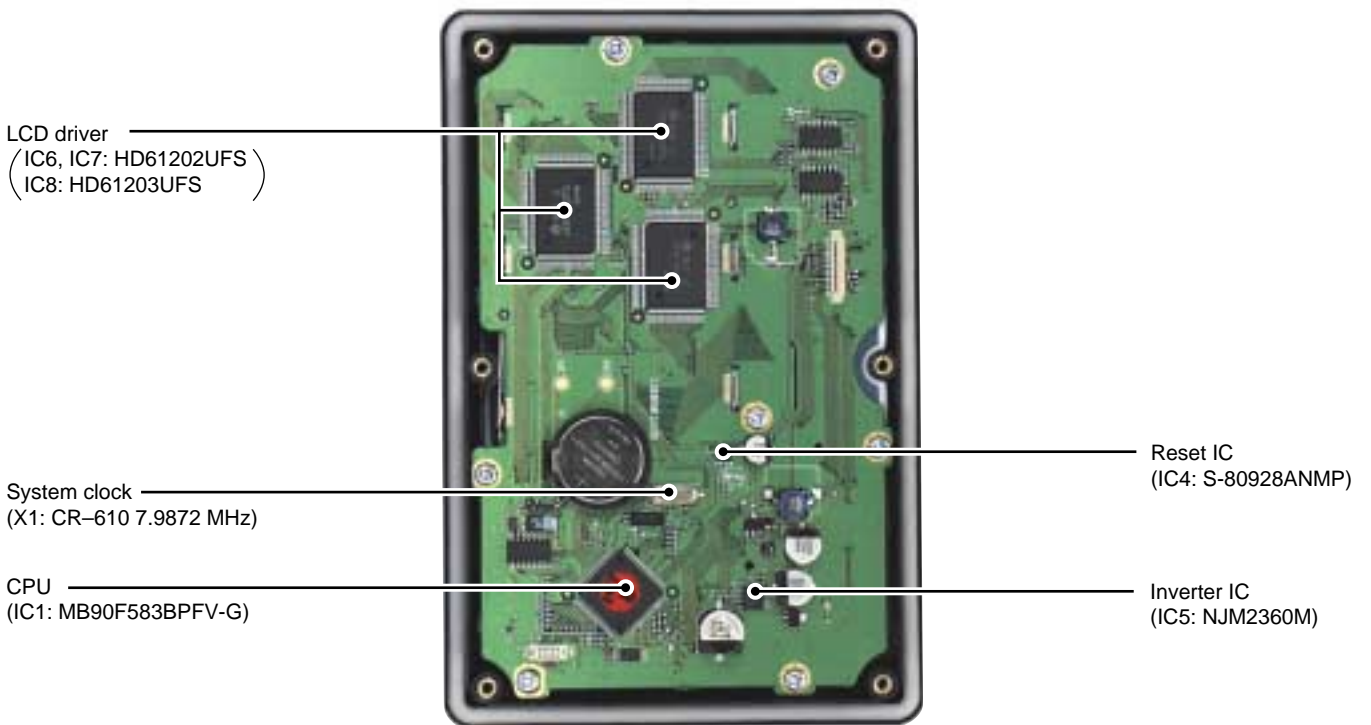
**All stated specifications are subject to change without notice or obligation.**

## SECTION 2 INSIDE VIEWS

### • MAIN UNIT



### • LOGIC UNIT



## SECTION 3 CIRCUIT DESCRIPTION

### 3-1 RECEIVER CIRCUITS

#### 3-1-1 RF AMPLIFIER CIRCUIT (MAIN UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna connector are amplified at the RF amplifier (Q1) via the bandpass filter (L1, C3). The amplified signals are applied to the 1st mixer circuit (Q2) after out-of-band signals are suppressed at the 3-stage of bandpass filters (L2, L3, L4, C11, C14, C16).

#### 3-1-2 1ST MIXER AND 1ST IF CIRCUITS (MAIN UNIT)

The 1st mixer circuit converts the received signal into a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through a crystal filter at the next stage of the 1st mixer.

The signals from the RF circuit are mixed at the 1st mixer (Q2) with a 1st LO signal coming from the PLL circuit to produce a 21.7 MHz 1st IF signal.

The 1st IF signal is applied to the crystal filters (F11, F12) to suppress out-of-band signals. The filtered 1st IF signal is amplified at the 1st IF amplifier (Q3), then applied to the 2nd mixer circuit (IC1, pin 16).

#### 3-1-3 2ND IF AND DEMODULATOR CIRCUITS (MAIN UNIT)

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC1, pin 16), and is mixed with the 2nd LO signal to be converted into a 450 kHz 2nd IF signal.

The FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 2nd LO signal (21.25 MHz) is produced at the PLL circuit using reference frequency.

The 2nd IF signal from the 2nd mixer (IC1, pin 3) passes through ceramic filter (F13) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC1, pin 5), and is applied to the quadrature detector (IC1, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

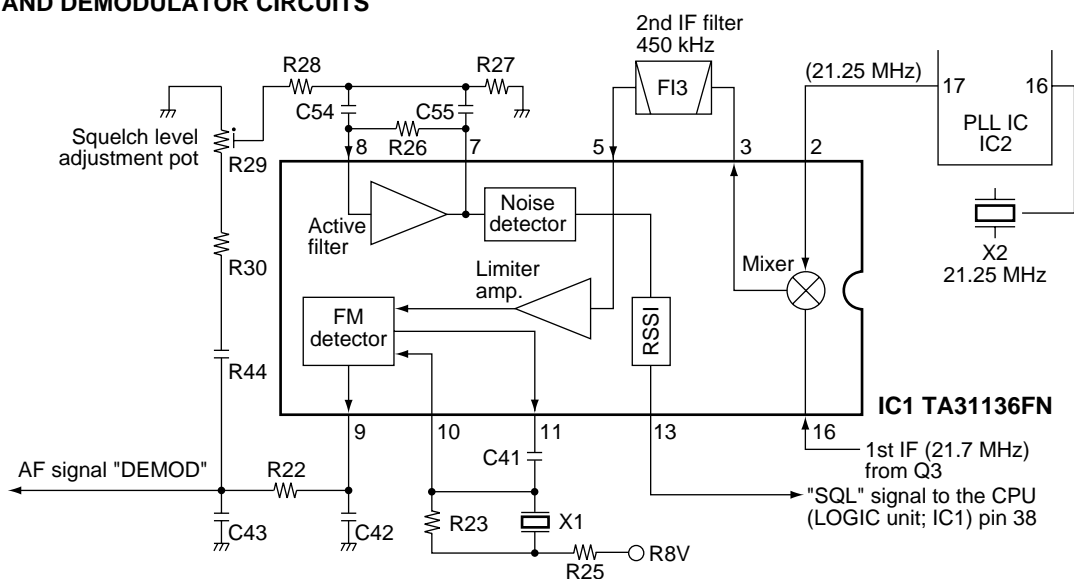
#### 3-1-4 SQUELCH CIRCUIT (MAIN UNIT)

A portion of the AF signals from the FM IF IC (IC1, pin 9) is applied to the active filter section (IC1, pin 8) where noise components are amplified and detected with an internal noise detector. The squelch level adjustment pot (R29) is connected to the active filter input (pin 8) to control the input noise level.

The active filter section amplifies noise components. The filtered signals are rectified at the noise detector section and converted into "SQL" signal (DC voltage) at the noise comparator section. The "SQL" signal is output from pin 13.

This squelch circuit is only used for the BUSY detection of Ch70, and is not related the DSC decoder sensitivity and etc.

#### •2ND IF AND DEMODULATOR CIRCUITS



## 3-2 PLL CIRCUIT

### 3-2-1 PLL CIRCUIT (MAIN UNIT)

A PLL circuit provides stable oscillation of the receiver 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL IC (IC2) contains a prescaler, programmable counter, programmable divider phase detector, charge pump and etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency (21.25 MHz).

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

## 3-3 DSC CIRCUITS

### 3-3-1 DSC DECODE CIRCUIT (MAIN UNIT)

The AF signals from FM IF IC (IC1, pin 9) are filtered at the bandpass filter (IC3A, pins 3, 1) with +18 dB/octave characteristics to remove except 1300 Hz and 2100 Hz signals. The filtered signals are converted analog signals into digital signals at IC4, and are then applied to the CPU after shaping waveform at IC6.

### 3-3-2 DSC ENCODE CIRCUIT (MAIN UNIT)

The DSC signals from the D/A outputs of CPU are amplified at the buffer amplifier (Q17) and converted into 600  $\Omega$  impedance at T1. The signals are output to the connected transceiver as floating system output.

## 3-4 NMEA AND DATA INTERFACE CIRCUITS

### 3-4-1 NMEA CIRCUIT (MAIN UNIT)

The NMEA signals (GGA) from OPC-945 are applied to IC5 and are shaped waveform at IC6, and are then applied to the CPU.

### 3-4-2 DATA INTERFACE CIRCUIT (MAIN UNIT)

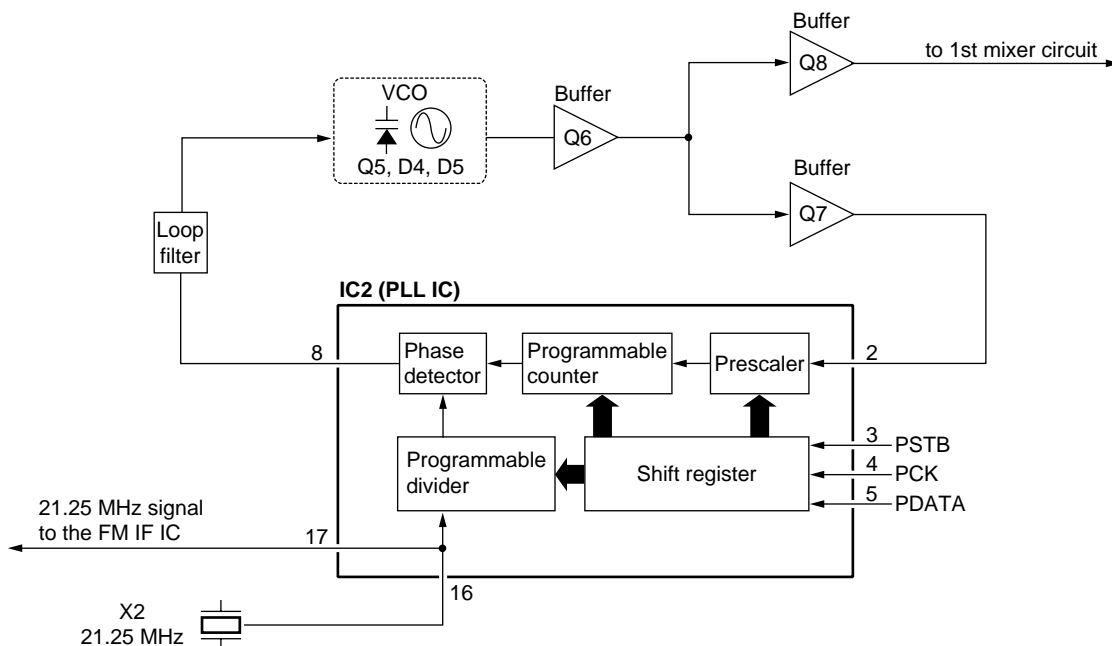
The control signals from the connected transceiver with OPC-951 are applied to IC8 and are shaped wave form at IC6, and are then applied to the CPU.

## 3-5 POWER SUPPLY CIRCUITS

### 3-5-1 VOLTAGE LINE (MAIN UNIT)

LINE	DESCRIPTION
Vcc	The voltage from the connected transceiver.
8 V	Common 8 V converted from the Vcc line and regulated by the 8 V regulator circuit (IC9).
5 V	Common 5 V converted from the 8 V line and regulated by the 5 V regulator circuit (IC10).
R8V	8 V for receiver circuits regulated by the R8V regulator circuit (Q15, Q16).

## • PLL CIRCUIT



### 3-6 LOGIC CIRCUITS (LOGIC UNIT)

#### • CPU

IC1 is 16 bit single chip microcomputer and contains serial I/O, timer, A/D converter, D/A converter, programmable I/O, ROM and RAM.

#### • SYSTEM CLOCK CIRCUIT

X1 is a high-stability crystal oscillator and oscillated a 7.9872 MHz system clock for the CPU (IC1).

#### • RESET CIRCUIT

IC4 is a reset IC. When turn power ON, IC4 outputs a reset signal ("LOW" pulse) to CPU (IC1, pin 75) via the RST line.

#### • LCD DRIVER

IC6–IC8 are LCD driver for a dot matrix LCD.

#### • INVERTER CIRCUIT

IC5 is a –8V DC-DC converter IC and converts –8 V from the HV line. The converted voltage (–8V) is used for driving the LCD.

#### • CLOCK CIRCUIT

IC3 is a clock IC and also used for backup the position/time information for DSC.

#### • DIMMER CIRCUIT

Q2, Q3, Q6 are dimmer circuit and control the LCD backlight (LED).

### 3-7 PORT ALLOCATIONS

#### 3-7-1 CPU (LOGIC UNIT)

Pin number	Port name	Description
1–7	KEY-3–KEY-9	Input port for the [3]–[9] keys.
8	KEY-0	Input port for the [0] key.
10	KEY-L	Input port for the [LEFT] key.
11	KEY-U	Input port for the [UP] key.
12	KEY-D	Input port for the [DOWN] key.
13	KEY-R	Input port for the [RIGHT] key.
14	KEY-A	Input port for the [A/a] key.
15	KEY-BS	Input port for the [BS] key.
19	CLR X	Input port for the cloning data from the buffer (MAIN unit; D8).
20	CLTX	Output port for the cloning data to the buffer (MAIN unit; Q9).
23	ECK	Outputs clock signal for EEPROM (IC2).
24	EDA	Outputs serial data signal for EEPROM (IC2).
26	RCEV	Outputs the R8V regulator circuit (MAIN unit; Q15, Q16) control signal. High : While receiving
30	DSMOD	D/A output port for the DSC encode signal to the buffer amplifier (MAIN unit; Q17).

Pin number	Port name	Description
31	CADJ	Outputs control signal for the LCD contrast.
36	NMEAI	Input port for serial signal from the NMEA connector (MAIN unit; J1) via the photo coupler (MAIN unit; IC5) and buffer amplifier (MAIN unit; IC6).
37	NMEAO	Outputs serial signal to the NMEA connector (MAIN unit; J1) via the buffer amplifier (Q13, Q14, D11).
38	SQL	Input port for noise level signal (DC voltage) for squelch operation.
41–44	DIM0–DIM3	Output LCD backlight control signals for the dimmer circuit (Q2, Q3, Q6).
45	DDEC	Input port for the DSC decode signal. Low : DSC signal is decoded.
46	UNLK	Input port for the PLL unlock signal. Low : While PLL is locked.
52, 53	CS1, CS2	Outputs chip select signal for the LCD drivers (IC6–IC8).
54, 55, 56	RW, DI, E	Output control signals for the LCD driver (IC6–IC8).
57	DATAS	Input port for the control signal from IC-M501EURO via the photo coupler (MAIN unit; IC8) and buffer amplifier (MAIN unit; IC6).
58	DATAM	Outputs the control signal to IC-M501EURO via the Buffer amplifier (MAIN unit; Q11, Q12, D10).
60	BUSY	Outputs busy LED (MAIN unit; DS1) control signal.
65	KEY-ENT	Input port for the [ENT] key.
66	KEY-CLR	Input port for the [CLR] key.
67	KEY-CAL	Input port for the [CALL] key.
68	KEY-DTR	Input port for the [DISTRESS] key.
69	BEEP	Outputs beep audio signal.
73	CCS	Outputs chip select signal for the clock IC (IC3).
74	PSTB	Outputs strobe signals for the PLL circuit.
83–90	DB0–DB7	Output data signals for the LCD driver (IC6–IC8).
96	SCK	Outputs clock signal to the clock IC (IC3).
97	SO	Outputs serial signal for the clock IC (IC3).
98	SI	Input port for serial signal from the clock IC (IC3).
99, 100	KEY-1, KEY-2	Input port for the [1], [2] keys.



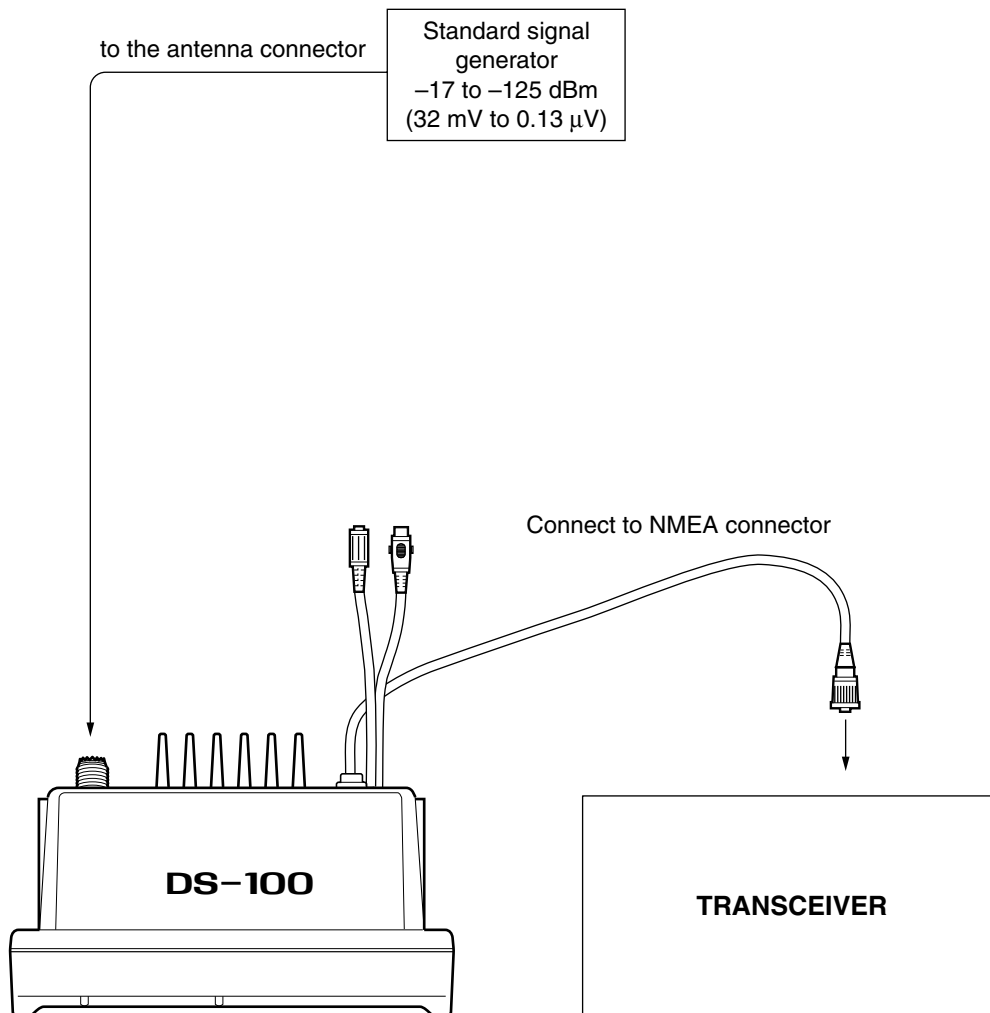
# SECTION 4 ADJUSTMENT PROCEDURES

## 4-1 PREPARATION

### ■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
TRANSCEIVER	Enable to connect to DS-100 (#02)	Digital multimeter	Measuring range : 10 mV–10 V
Frequency counter	Frequency range : 0.1–300 MHz	DC voltmeter	Input impedance : 50 k $\Omega$ /V DC or better
	Frequency accuracy: $\pm 1$ ppm or better		
Standard signal generator (SSG)	Sensitivity : 100 mV or better	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
	Frequency range : 0.1–300 MHz	Terminator	Impedance : 100 k $\Omega$ Capacity : 5 W or more
Output level : 0.1 $\mu$ V–32 mV (–127 to –17 dBm)			

### ■ CONNECTIONS

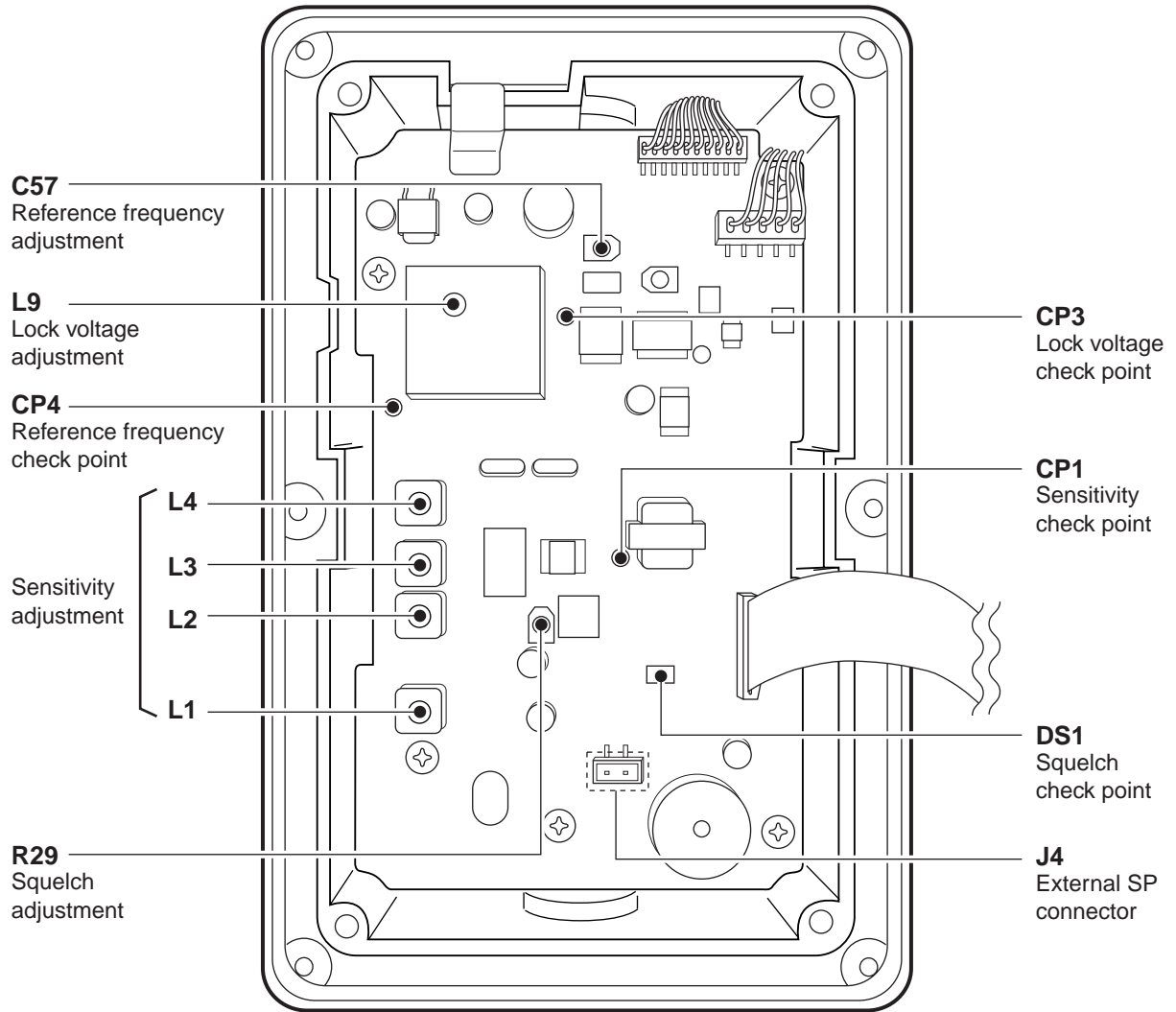


## 4-2 REFERENCE AND RECEIVER ADJUSTMENTS

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
		UNIT	LOCATION		UNIT	ADJUST
LOCK VOLTAGE	1 • Receiving	MAIN	Connect a digital multi-meter or oscilloscope to check point CP3.	2.1 V	MAIN	L9
REFERENCE FREQUENCY	1 • Receiving	MAIN	Connect a frequency counter to check point CP4.	134.825000 MHz	MAIN	C57
SENSITIVITY	1 • Connect a 100 k $\Omega$ dummy load to the external speaker jack J4 on MAIN unit. • Connect an SSG to the antenna connector and set as: Frequency : 156.525 MHz Level : 10 $\mu$ V* (-97 dBm) Modulation : 1 kHz Deviation : $\pm$ 3.0 kHz • Receiving	MAIN	Connect a digital multi-meter or oscilloscope to check point CP1.	Maximum voltage	MAIN	L1, L2, L3, L4
SQUELCH	1 • Turn R29 counter clockwise on the MAIN unit to 9 o'clock position. • Connect an SSG to the antenna connector and set as: Frequency : 156.525 MHz Level : 0.25 $\mu$ V* (-119 dBm) Modulation : 1 kHz Deviation : $\pm$ 3.0 kHz • Receiving	MAIN	DS1	At the point where the check point DS1 just turns OFF.	MAIN	Turn R29 to clockwise.

\*This output level of a standard signal generator (SSG) is indicated as SSG's open circuit.

• MAIN UNIT









[MAIN UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.
C83	4030007020	S.CERAMIC C1608 CH 1H 120J-T	T
C84	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C85	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C86	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C87	4030008850	S.CERAMIC C1608 JB 1H 123K-T	T
C88	4030008900	S.CERAMIC C1608 JB 1H 333K-T	T
C89	4030008900	S.CERAMIC C1608 JB 1H 333K-T	T
C90	4030006850	S.CERAMIC C1608 JB 1H 471K-T	T
C91	4030008920	S.CERAMIC C1608 JB 1H 473K-T	T
C92	4030011810	S.CERAMIC C1608 JB 1A 224K-T	T
C93	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C94	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C95	4510004630	S.ELECTROLYTIC ECEV1CA100SR	T
C96	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C97	4340000310	S.MYLAR ECHU 1C 333JX5	T
C98	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C99	4030006870	S.CERAMIC C1608 JB 1H 222K-T	T
C100	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C101	4030006880	S.CERAMIC C1608 JB 1H 472K-T	T
C102	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C103	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C104	4030006850	S.CERAMIC C1608 JB 1H 471K-T	T
C106	4030006880	S.CERAMIC C1608 JB 1H 472K-T	T
C107	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C108	4030007090	S.CERAMIC C1608 CH 1H 470J-T	T
C109	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C110	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C111	4510004590	ELECTROLYTIC 16 MV 470 HC	T
C112	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C113	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C114	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C115	4510004630	S.ELECTROLYTIC ECEV1CA100SR	T
C116	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C117	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C118	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C119	4510004630	S.ELECTROLYTIC ECEV1CA100SR	T
C120	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C121	4030007090	S.CERAMIC C1608 CH 1H 470J-T	T
C123	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C124	4550006150	S.TANTALUM ECST1CY105R	T
C126	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C127	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C130	4030012600	S.CERAMIC C2012 JB 1A 105M-T	T
C131	4550006130	S.TANTALUM ECST1VY224R	T
C132	4030008890	S.CERAMIC C1608 JB 1H 273K-T	T
C133	4030008890	S.CERAMIC C1608 JB 1H 273K-T	T
C134	4030006870	S.CERAMIC C1608 JB 1H 222K-T	T
C135	4030009490	S.CERAMIC C1608 JB 1H 821K-T	T
C136	4510004630	S.ELECTROLYTIC ECEV1CA100SR	T
C137	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C138	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C139	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C140	4510004630	S.ELECTROLYTIC ECEV1CA100SR	T
C141	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C142	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C143	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C144	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C145	4030007030	S.CERAMIC C1608 CH 1H 150J-T	T
C146	4030007030	S.CERAMIC C1608 CH 1H 150J-T	T
C147	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C148	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C149	4030011600	S.CERAMIC C1608 JB 1E 104K-T	T
C150	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C151	4030006900	S.CERAMIC C1608 JB 1H 103K-T	T
C152	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C153	4030006860	S.CERAMIC C1608 JB 1H 102K-T	T
C154	4550006830	S.TANTALUM ECST1DY475R	T
C155	4030009490	S.CERAMIC C1608 JB 1H 821K-T	T
C156	4030006870	S.CERAMIC C1608 JB 1H 222K-T	T
C157	4510004630	S.ELECTROLYTIC ECEV1CA100SR	T
J1	6510022310	S.CONNECTOR B5B-PH-SM3-TB	T
J2	6510022030	S.CONNECTOR B10B-ZR-SM3-TF	T
J3	6510019500	S.CONNECTOR 52559-2290	T
J4	6510003380	CONNECTOR B02B-EH-S	T
DS1	5040002310	S.LED SML-311YTT86	T
T1	5920000570	TRANSFORMER 12T01	T
SP1	2520000110	PIEZO BUZZER PS1740P02	T
EP1	0910052945	PCB B 5473E	T

[CHASSIS UNIT]

REF NO.	ORDER NO.	DESCRIPTION	M.
J1	6510004880	CONNECTOR MR-DS-E 01	
W1	8900009740	CABLE OPC-945 <CMI>	
W2	8900010690	CABLE OPC-1088 <LIA>	
W3	7120000470	JUMPER ERDS2T0	
EP1	6910011940	BEAD ZCAT2436-1330A-BK-M	

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)

S.=Surface mount

## SECTION 6 MECHANICAL PARTS

### [CHASSIS PARTS]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6510004880	Connector MR-DS-E 01	1
W1	8900009740	Cable OPC-945	1
W2	8900009690	Cable OPC-951	1
EP1	6910011940	Bead ZCAT2436-1330A-M	1
MP3	8410002341	2349 heatsink-1	1
MP4	8210017200	2349 front panel assembly	1
MP5	8210017150	2345 rear panel assembly	1
MP6	8930052060	2345 F-packing	1
MP7	8930052050	2345 R-packing	1
MP16	8930052430	2345 A-IC clip	1
MP18	8810008660	Screw PH B0 M3 × 8 NI-ZU (BT)	5
MP19	8810008660	Screw PH B0 M3 × 8 NI-ZU (BT)	7
MP20	8810004540	Screw M3 × 8 SUS	6
MP21	8810006050	Icom screw E7	6
MP22	8930052290	O ring (AD)	6
MP23	8850000690	Flat washer M3 (3×7×0.5) SUS	6
MP25	8810004540	Screw M3 × 8 SUS	2
MP26	8930034300	1542 ANT seal	1
MP27	8930049320	2288 VENT. sheet	1

### [MAIN UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
SP1	2520000110	Piezo buzzer PS1740P02	1
MP1	8510012590	2289 VCO case	1

### [LOGIC UNIT]

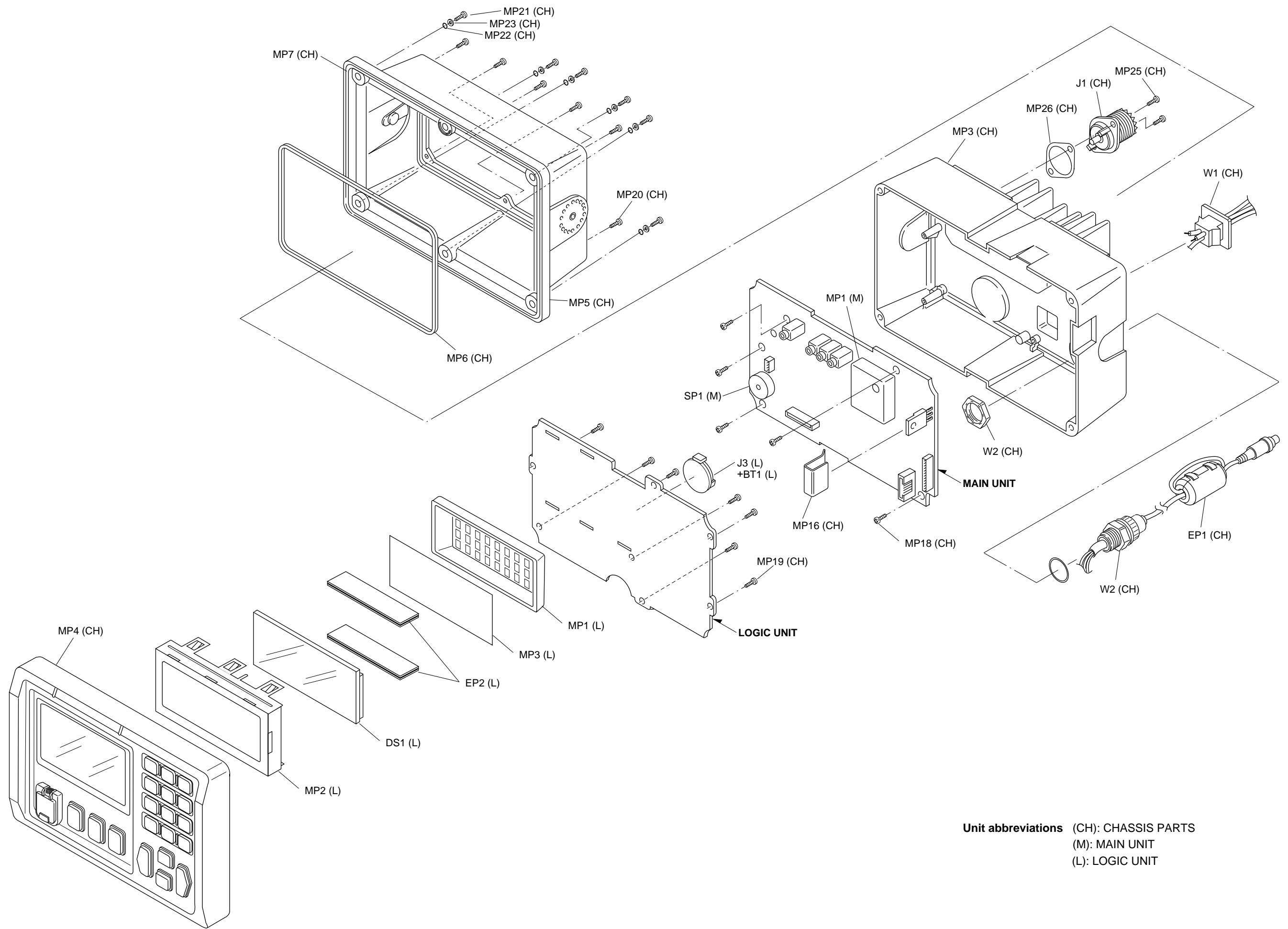
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J3	6510021860	Connector BH-800.8	1
BT1	3020000110	Lithium CR2032	1
DS1	5030001850	LCD TSD0402-UFFDCW	1
EP2	8930052541	LCD contact SRCN-2349-SP-N-W-2	2
MP1	8210016790	2349 reflector	1
MP2	8930051950	2349 LCD holder	1
MP3	8930052530	2349 LCD filter	1

### [UNPACKING]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
MP1	8610010560	2040 knob bolt (black)	2
MP2	8010018151	2345 mobile bracket-1	1
MP3	8850000500	Spring washer M5 SUS	2
MP4	8810001490	Screw PH A M5 × 20 SUS	2
MP5	8850000180	Flat washer M5 SUS	2

**Screw abbreviations** PH: Pan head B0, BT: Self-Tapping  
 SUS: Stainless NI-ZU: Nickel-zinc

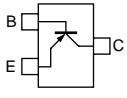
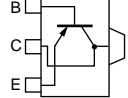
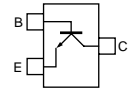
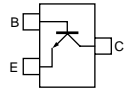
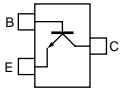
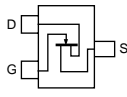
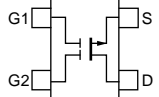
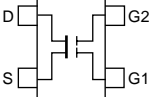
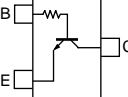
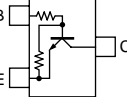




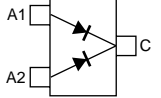
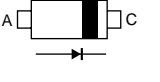
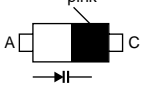
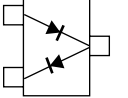
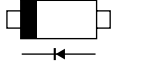
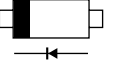
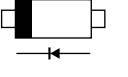
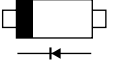
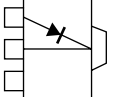
**Unit abbreviations** (CH): CHASSIS PARTS  
(M): MAIN UNIT  
(L): LOGIC UNIT

# SECTION 7 SEMI-CONDUCTOR INFORMATION

## • TRANSISTORS AND FET'S

<b>2SA1362 GR</b> (Symbol: AEG) 	<b>2SB1132 R</b> (Symbol: BAR) 	<b>2SC2714 Y</b> (Symbol: QY) 	<b>2SC4116 BL</b> (Symbol: LL) 	<b>2SC4215 O</b> (Symbol: QO) 
<b>2SK210 GR</b> (Symbol: YG) 	<b>3SK206</b> (Symbol: U78) 	<b>3SK292</b> (Symbol: UK) 	<b>DTC144 TU</b> (Symbol: 06) 	<b>RN1404</b> (Symbol: XD) 

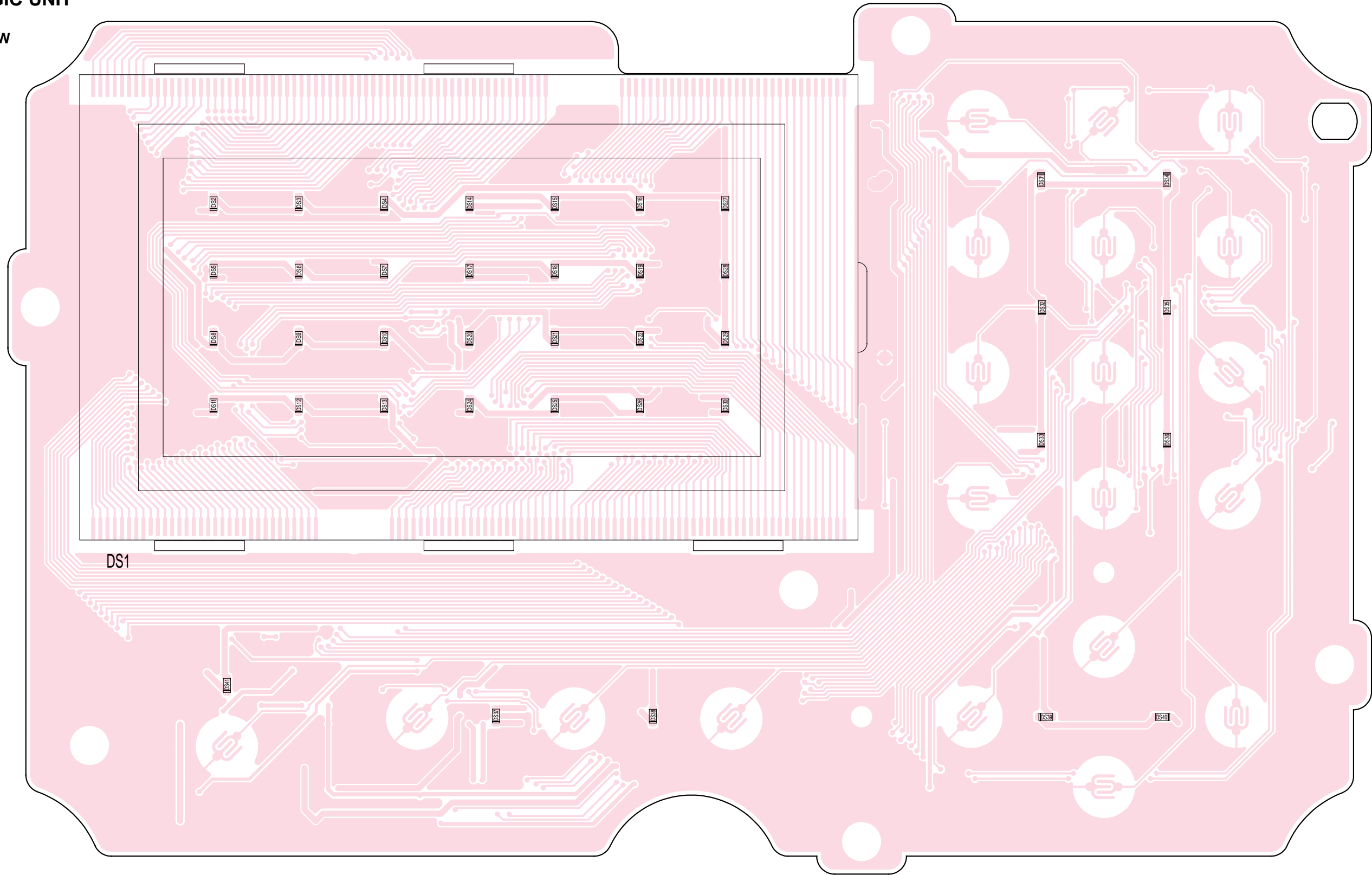
## • DIODES

<b>1SS184</b> (Symbol: B3) 	<b>1SS355</b> (Symbol: A) 	<b>1SV214</b> (Symbol: T1) 	<b>DA204 U T107</b> (Symbol: K) 	<b>HSU88TRF</b> (Symbol: 9) 
<b>MA8036 L</b> (Symbol: 3_6) 	<b>MA8043 L</b> (Symbol: 4_3) 	<b>MA8056 M</b> (Symbol: 5-6) 	<b>SB10 05PCP TD</b> (Symbol: SA) 	

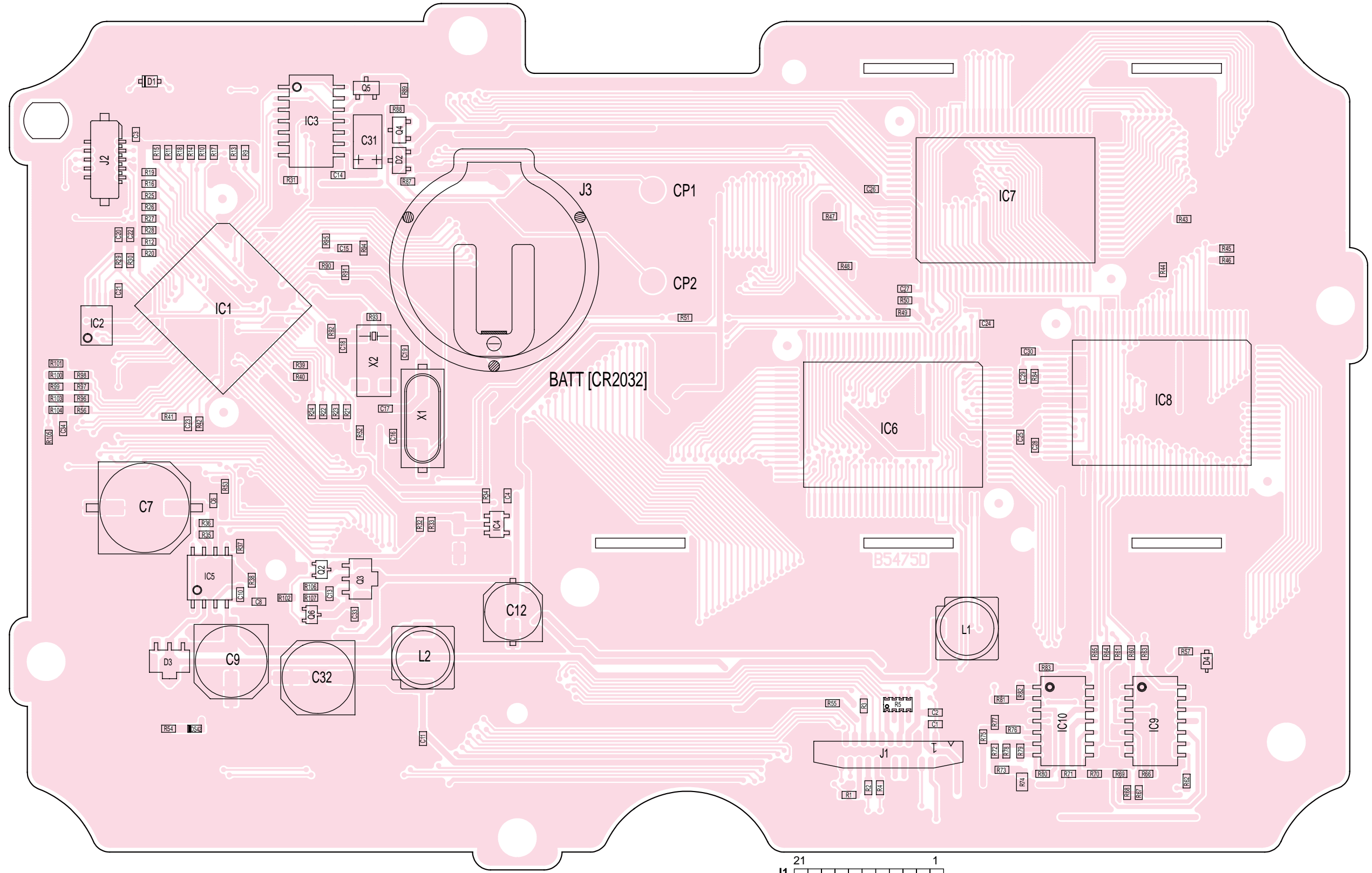
# SECTION 8 BOARD LAYOUTS

## 8-1 LOGIC UNIT

• TOP VIEW



• BOTTOM VIEW

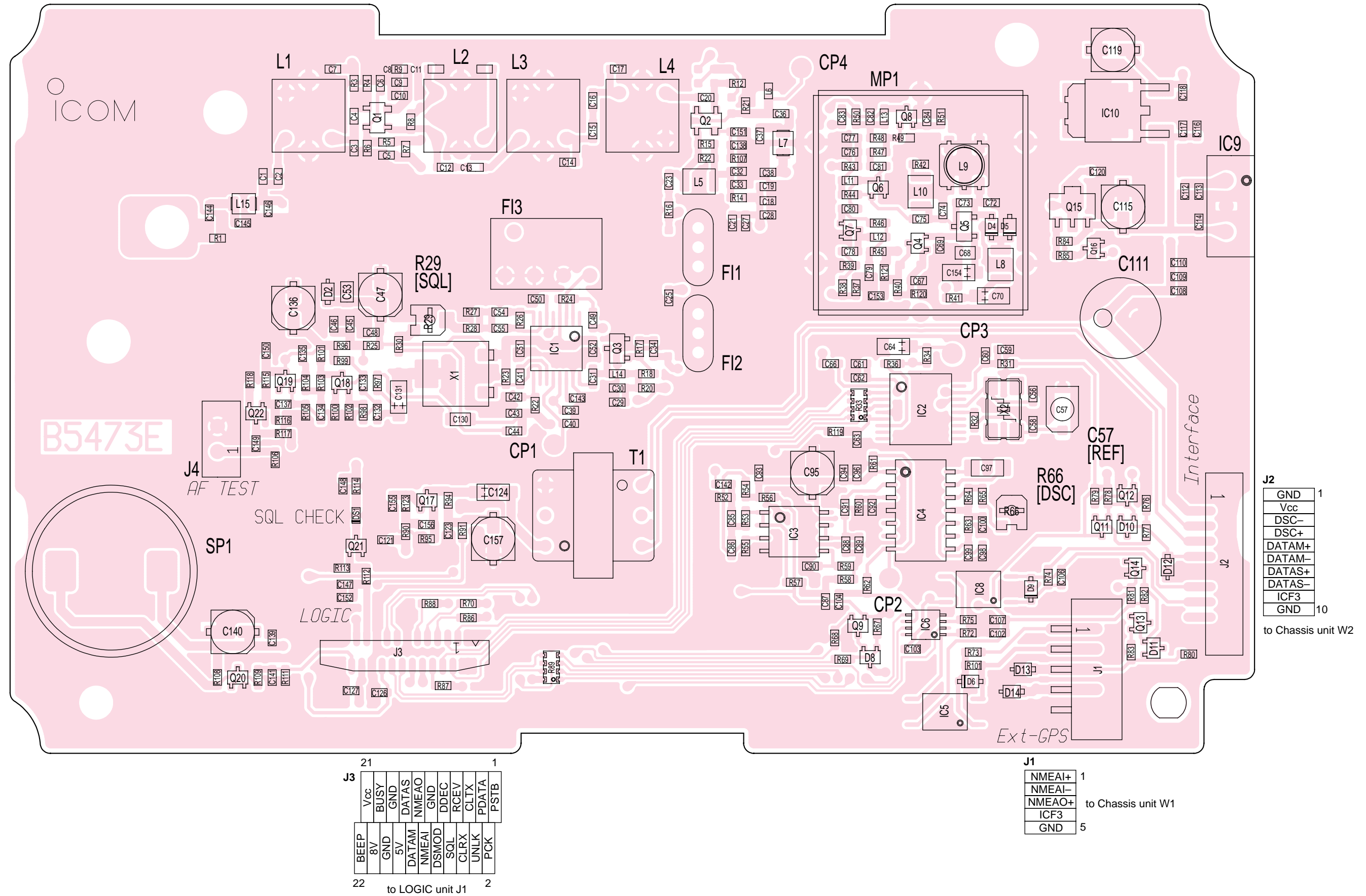


21	PCK	1
	UNLK	
	CLR X	
	SQL	
	DSMOD	
	NMEAI	
	DATAS	
	5V	
	GND	
	BUSY	
	8V	
	Vcc	
22	BEEP	2

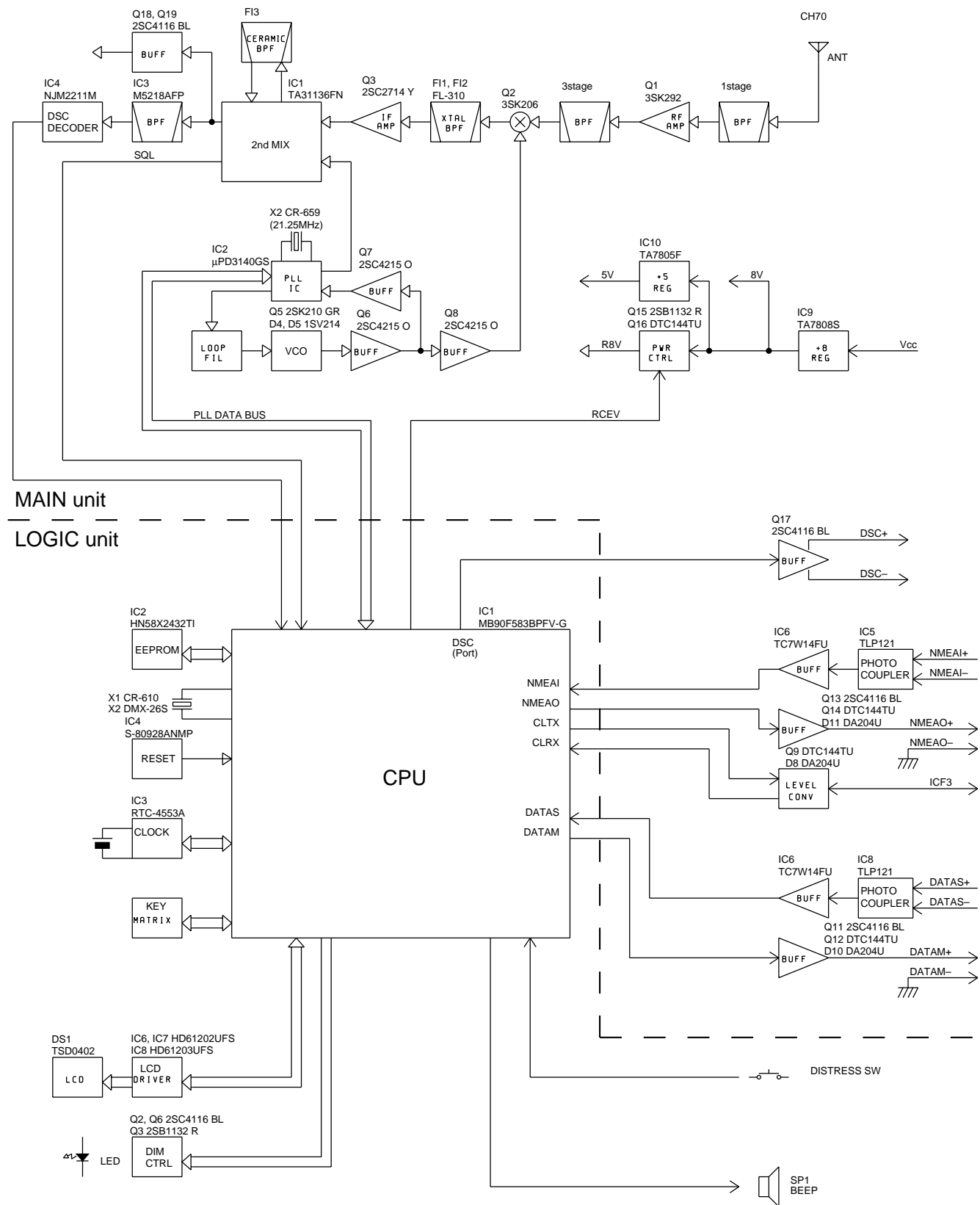
to MAIN unit J3

# 8-2 MAIN UNIT

• TOP VIEW

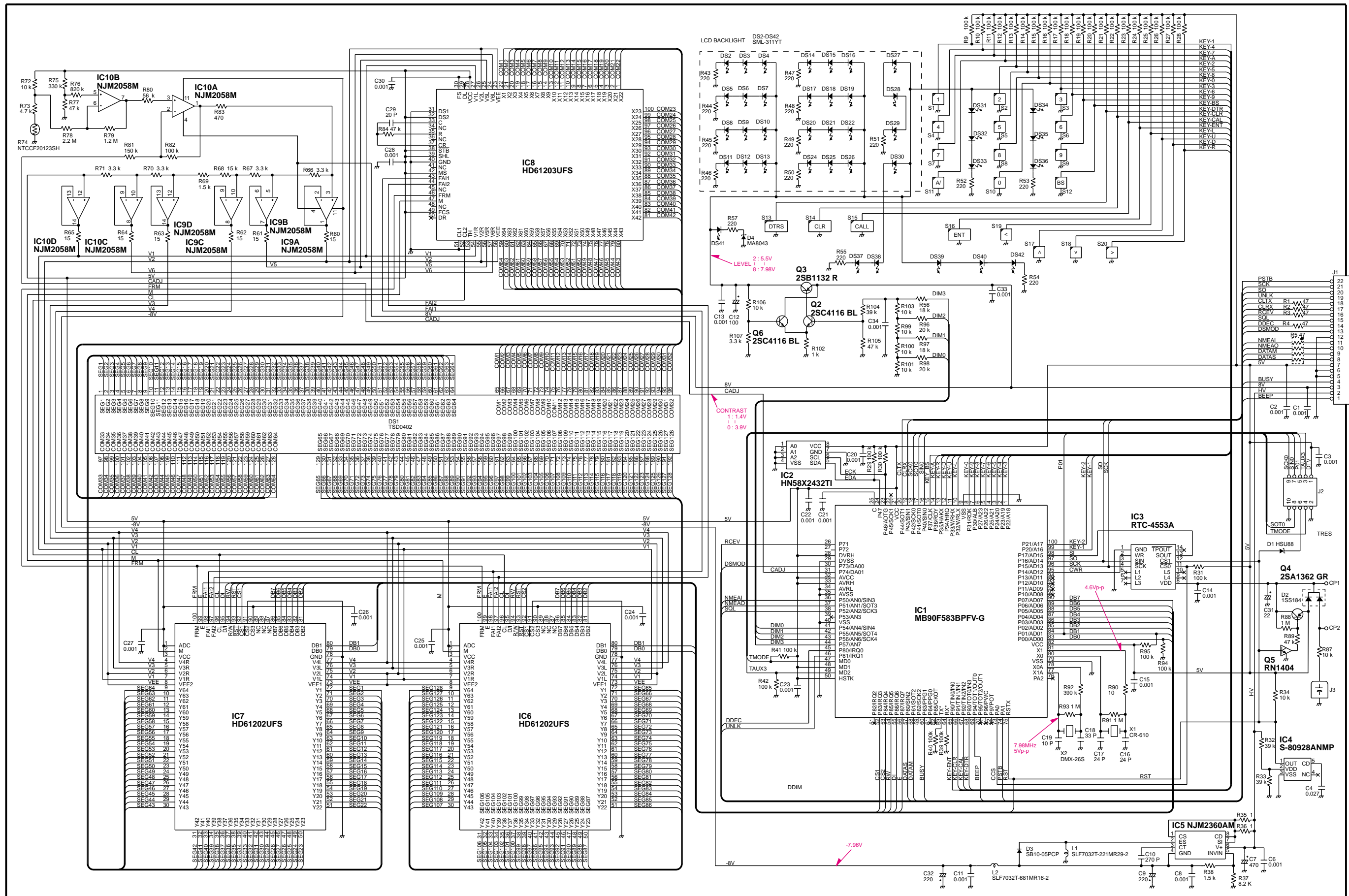


# SECTION 9 BLOCK DIAGRAM

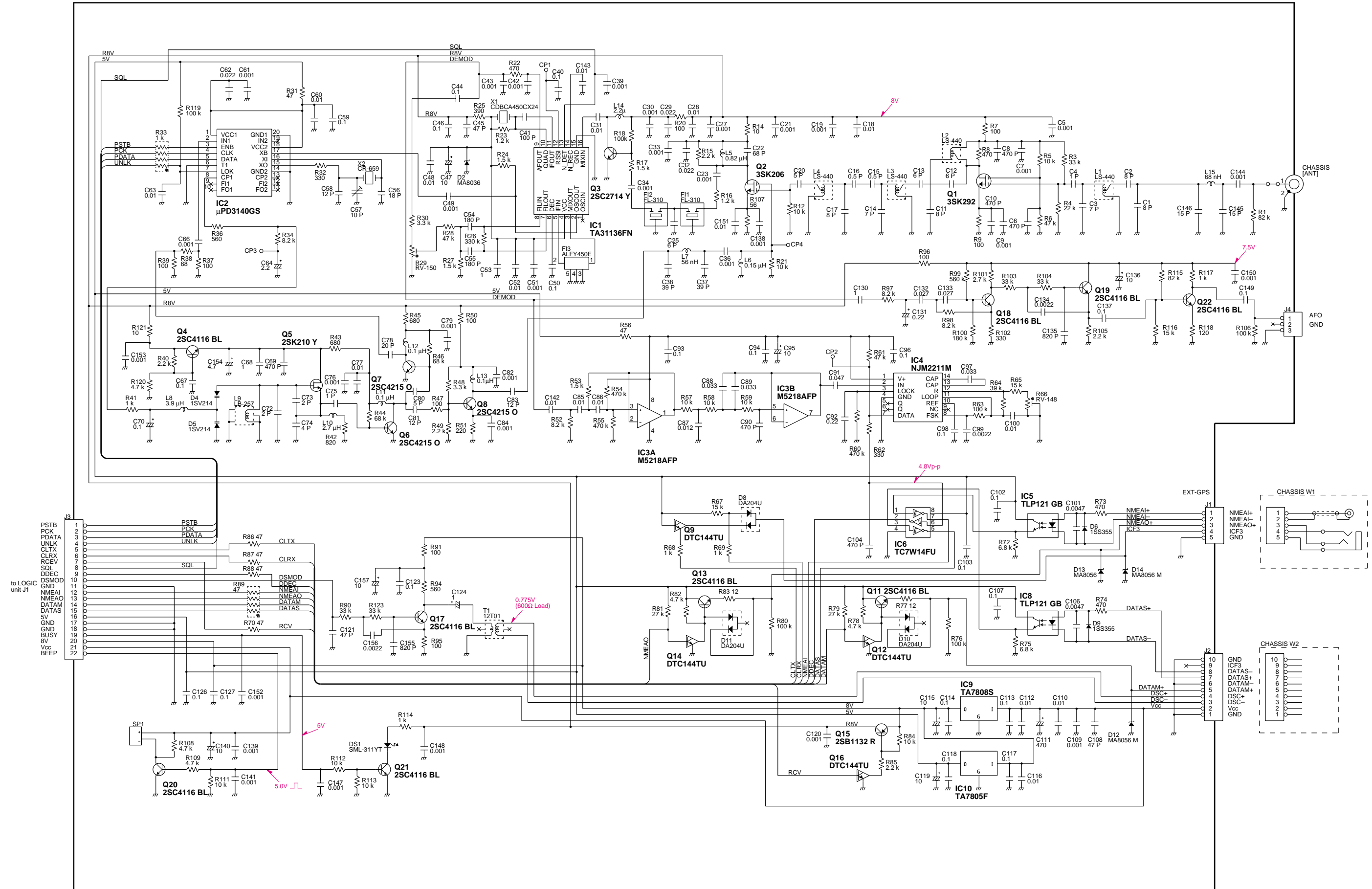


# SECTION 10 VOLTAGE DIAGRAM

## 10-1 LOGIC UNIT



10-2 MAIN UNIT





## Icom Inc.

1-1-32, Kamiminami, Hirano-ku, Osaka 547-0003, Japan

Phone : +81 (06) 6793 5302

Fax : +81 (06) 6793 0013

URL : <http://www.icom.co.jp/world/index.html>

### Icom America Inc.

<Corporate Headquarters>

2380 116th Avenue N.E., Bellevue, WA 98004, U.S.A.

Phone : +1 (425) 454-8155 Fax : +1 (425) 454-1509

URL : <http://www.icomamerica.com>

<Customer Service>

Phone : +1 (425) 454-7619

### Icom Canada

Glenwood Centre #150-6165

Highway 17 Delta, B.C., V4K 5B8, Canada

Phone : +1 (604) 952-4266 Fax : +1 (604) 952-0090

URL : <http://www.icomcanada.com>

### Icom (Australia) Pty. Ltd.

A.B.N. 88 006 092 575

290-294 Albert Street, Brunswick, Victoria, 3056, Australia

Phone : +61 (03) 9387 0666 Fax : +61 (03) 9387 0022

URL : <http://www.icom.net.au>

### Icom New Zealand

146A Harris Road, East Tamaki,

Auckland, New Zealand

Phone : +64 (09) 274 4062 Fax : +64 (09) 274 4708

URL : <http://www.icom.co.nz>

### Beijing Icom Ltd.

1305, Wanshang Plaza, Shijingshan Road, Beijing China

Phone : +86 (010) 6866 6337 Fax : +86 (010) 6866 3553

URL : <http://www.bjicom.com>

### Icom (Europe) GmbH

Communication Equipment

Himmelgeister Str. 100, D-40225 Düsseldorf, Germany

Phone : +49 (0211) 346047 Fax : +49 (0211) 333639

URL : <http://www.icomeurope.com>

### Icom Spain S.L

Crta. de Gracia a Manresa Km. 14,750

08190 Sant Cugat del Valles Barcelona, SPAIN

Phone : +34 (93) 590 26 70 Fax : +34 (93) 589 04 46

URL : <http://www.icomspain.com>

### Icom (UK) Ltd.

Unit 9, Sea St., Herne Bay, Kent, CT6 8LD, U.K.

Phone : +44 (01227) 741741 Fax : +44 (01227) 741742

URL : <http://www.icomuk.co.uk>

### Icom France S.a

Zac de la Plaine, 1, Rue Brindejonc des Moulinais

BP 5804, 31505 Toulouse Cedex, France

Phone : +33 (5) 61 36 03 03 Fax : +33 (5) 61 36 03 00

URL : <http://www.icom-france.com>

### Asia Icom Inc.

6F No. 68, Sec. 1 Cheng-Teh Road, Taipei, Taiwan, R.O.C.

Phone : +886 (02) 2559 1899 Fax : +886 (02) 2559 1874

URL : <http://www.asia-icom.com>

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